The Fiber Road Card

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STT Meeting

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SCL Init

Monitoring and L3 Requests

VME Interrupt vs Dedicated line

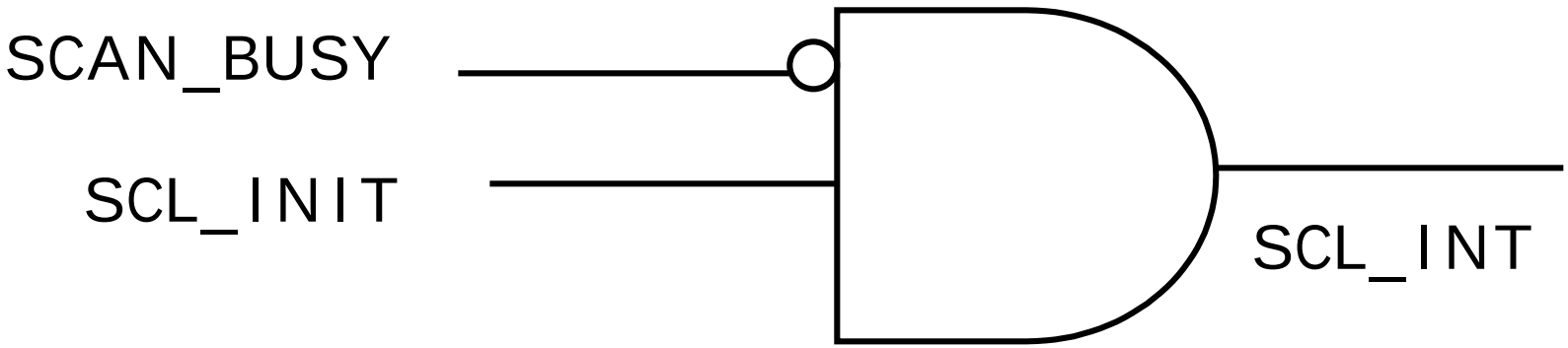
Connector Test

Track Truncation Study

SCL Init at SCLF

1. INIT_SECTION asserted on input
2. Disable latching SCL data to SCLF
3. Set INIT_ACK to SCL mezzanine
4. Wait for SCAN_BUSY to clear
5. Send SCL_INIT signal to CPU (on dedicated line or via VME interrupt)
6. Wait for INIT_DONE from CPU (VME Register in SCLF)
7. Enable latching SCL data to SCLF
8. Clear L1_ERROR and L2_ERROR in SCLCR
9. Clear INIT_ACK to SCL mezzanine

SCL INIT Request to CPU



SCL Init at CPU

1. Write SCL_READY[i] signal bits to each VME memory register (BC, DB, MB)
2. Receive SCL_DONE[i] from each elements (poll)
3. Acknowledge by clearing SCL_READY[i] signal bit in all BC and DB VME memory registers
4. Wait for all units to Receive SCL_INIT from SCLF/FRC
5. acknowledge (Units clear SCL_DONE[i])
6. Send INIT_DONE to SCLF

SCL Init at Component

1. Each Component receives SCL_READY[i] from CPU
2. Input elements (RR) clear data
   a) Disable latching input data
   b) Wait n clock cycles w/o valid data
   c) Enable latching input data
3. Processing elements (SCLF, TRDF) reset inputs
   a) Reset Input FIFOs

SCL Init at Component Cont.

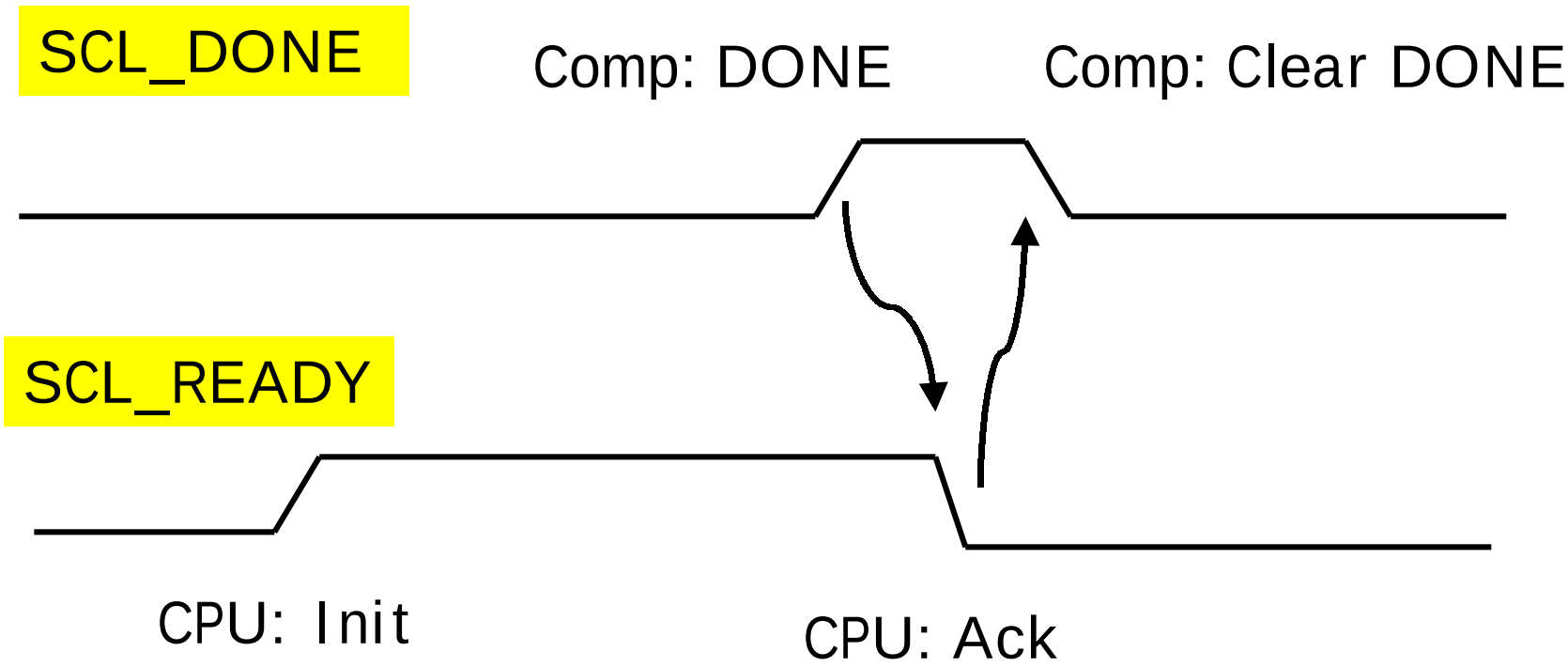
4. Buffer Manager reset inputs
   a) Reset Input FIFOs
   b) Mark all buffers as unused
5. Reset all Control/Status/Monitoring registers (except SCL_INIT registers)
6. Each Component sets SCL_DONE[i]
7. Wait for CPU to Clear SCL_READY[i]
8. Clear SCL_DONE[i]

SCL init handshaking

Action	SCL_DONE[i]	SCL_READY[i]
SCL_READY	0	0
CPU: SCL_INIT	0	1
Component inits	0	1
Component done	1	1
CPU ACK	1	0
Component CLEARS DONE	0	0
Ready	0	0

SCL handshaking between CPU and components.

SCL init handshaking



SCL handshaking between CPU and components.

Questions

- Since all reset requests are sent in parallel now, what about elements where the order matters: (i.e. road receivers before formatters)
- Solutions:
  - The CPU could enforce the order by only sending the init request to a unit after it gets the INIT_DONE from the previous one.
  - The daughter boards handle the sequence by communicating with each other (not great)

Questions

- What to send out to L3 upon SCL_INIT
  a. Kill everything, send nothing
  b. Finish current event, but dump everything afterwards
  c. Keep all events before the one with the SCL init
  - In b and c, SCLF has to know the state of the system

Possible: State known via VBD_BUSY from BM

- SCLF only sends SCL_INIT request to CPU if VBD is done

Or CPU could know about state of VBD (not so good).

Questions

Jim: The event the SCL init corresponds to and all up to 15 previous ones in the buffers can be thrown away: a) is fine.

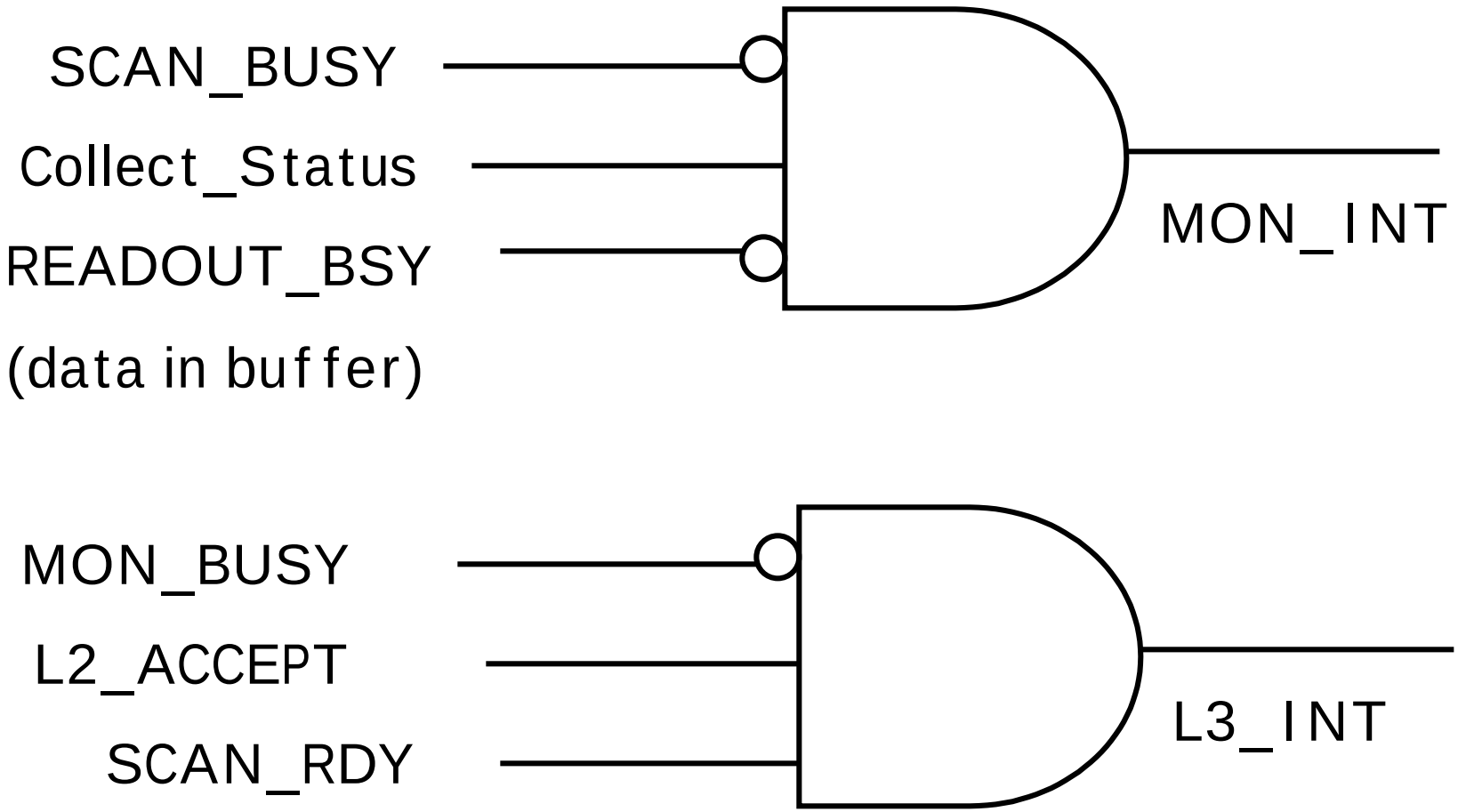
- What kind of monitoring data should be send after SCL init?

Jim: Don't need to send any, just start over.

- VME interrupt versus dedicated line. What if an SCL init request comes while VME is busy (i.e. VBD uses it for several hundred μs or even ms?

- Wait until VBD releases VME
- Since nothing needs to be monitored /saved, the SCL init could come as a VME interrupt (highest priority) at any time the bus is released

Monitoring and L3 Requests to CPU



Monitoring Requests at the FRC

1. Receive Collect_Status
2. Wait for all data in Buffer (poll READOUT_BUSY*)
3. Wait for VBD to released VME (poll SCAN_BUSY*)
4. Send Monitoring request to CPU (MON_INIT)
5. Wait for MON_DONE from CPU

L3 Requests at the FRC

1. Receive L2_Accept
2. Wait for all data in Out FIFO (poll SCAN_READY)
3. Wait for Monitoring to be done (poll MON_BUSY*)
4. Send L3 request to CPU (L3_INIT)
5. Wait for L3_DONE from CPU

Connector Test

- An Qi laid out test board including holes for stand-off
- Connection can be tested using only two pins per connector
- Received quote from a company

Truncation Study

- Use mc_exam:
- Includes info for

Cal (Calorimeter digi), CFT, CPS, FPS, MET, Jets, Kine (generated event), Muon, SMT, Reco Track, Vergen (Vertex)

- Tested, Runs on 1.1 av Min Bias events, but crashes on fixed N(Min Bias)???
- Use Root ntuples
- Writing macro to do truncation and implement triggers
- Summer student June 5, stay tuned!

What Next

- Finish Truncation Study by the end of summer
- Understand VRB/VRBC protocol and determine if we can adopt it for BM/BC communication
- Understand all buffering stages: FIFO depths, timing requirements